



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/768,668

01/30/2004

Yutaka Saeki

NEM-05301

8256

26339 7590 07/27/2010
MUIRHEAD AND SATURNELLI, LLC
200 FRIBERG PARKWAY, SUITE 1001
WESTBOROUGH, MA 01581

EXAMINER

SITTA, GRANT

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

07/27/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/768,668 | SAEKI, YUTAKA | |
| | Examiner | Art Unit | |
| | GRANT D. SITTA | 2629 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,6,7,25,28 and 29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,6,7,25,28 and 29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 6-7, 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Yatabe et al (6,188,395) hereinafter, Yatabe.

4. In regards to claim 1, AAPA teaches a current-drive apparatus for a display panel, comprising: a plurality of current-drive circuits (fig. 1 (section for 2a and 2b)), each of said plurality of current-drive circuits including first (fig. 1 Terminal at VDD and R1) and second terminals (fig. 1 Terminal A),

AAPA fails to teach a reference resistor connected between said first and second terminals and a reference current generation circuit to produce at least one internal reference current responding to a voltage generated based on the reference resistor

However Yatabe teaches a reference resistor connected between said first and second terminals (**fig. 1 (R1-R5)**) and a reference current generation circuit to produce at least one internal reference current responding to a voltage generated (col. 7, lines 1-67 $V_a = (V_{DD} + V_{EE})/2 = V_o$) based on the reference resistor (col. 12, lines 15-20).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA to include the use of a reference resistor as taught by Yatabe such that it is possible for the electric potential difference between the two driving electric potentials which are supplied to the output circuit to be reduced more than the electric potential difference between a first electric potential and a second electric potential, and consequently, it is possible to reduce the voltage resistance of the circuit device of the output circuit, and also to reduce the power consumption via the output circuit" as stated in (col. 4, lines 37-43 of Yatabe).

Therefore, AAPA as modified by Yatabe teaches a current source (fig. 1 (5) AAPA), said current source and said plurality of current-drive circuits being connected such that a current flowing through said current source becomes substantially equal to a current flowing through said reference resistor of each of said current-drive circuits (col. 7, lines 22-35), wherein a current flowing through said reference resistor in a first one of said current-drive circuits flows through (col. 7, lines 28 Yatabe) said reference resistor in a second one of said current-drive circuits (fig. 1 A and A' Yatabe),

wherein said current drive circuits are coupled in series (fig. 1 1, 2, 3, 4 are in series AAPA) in a manner that said first terminal of a preceding one of said current drive circuits is connected to the second terminal of a succeeding one of said current-drive circuits (fig. 1 4, 3, 2, 1 are connected though not directly connected AAPA) which is adjacent to the preceding one of said current-drive circuits ([0007-0009] AAPA)), and

wherein at least one of said plurality of current-drive circuits further includes at least one current adjustment resistor (fig. 1 (R8-R11 col. 7, lines 10-20 *"[t]he output side of the operational amplifiers OP1, OP2, OP3 and OP4 are connected to resistors R8, R9, R10 and R11, respectively, and the resistors R8 through R11 restrict the output current of the operational amplifiers OP1 through OP4"*) and wherein said at least one current adjustment resistor operates such that a reference voltage generated based on a voltage at both ends of said reference resistor is applied across said at least one current adjustment resistor to generate said at least one internal reference current (col. 8, lines 25-31 Yatabe).

5. In regards to claim 25, AAPA teaches a current-drive system for a display panel, comprising ([0007-0010] AAPA): first (fig. 1 (VDD)) and second power source lines (fig. 1 (5)); a plurality of current-drive ICs (fig. 1 4,3,2,1)), each of said plurality of current-drive ICs having first and second terminals (fig. 1 nodes connection ICs)

AAPA fails to teach having a first resistor connected between said first and second terminals.

Art Unit: 2629

However Yatabe teaches having a first resistor connected between said first and second terminals;**(fig. 1 (R1-R5))** (col. 7, lines 30-35 $V_a = (V_{DD} + V_{EE})/2 = V_o$) (col. 12, lines 15-20).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA to include the use of a first resistor connected between said first and second terminals as taught by Yatabe in order to make “possible for the electric potential difference between the two driving electric potentials which are supplied to the output circuit to be reduced more than the electric potential difference between a first electric potential and a second electric potential, and consequently, it is possible to reduce the voltage resistance of the circuit device of the output circuit, and also to reduce the power consumption via the output circuit” as stated in (col. 4, lines 37-43 of Yatabe).

Therefore, AAPA as modified by Yatabe teaches a current source connected to said plurality of current-drive ICs so that said ICs and said current source are connected in cascade with said first and second terminals between first and second power source lines ([007-0010] (fig. 1 VDD cascaded 1,2,3,4 and (5) AAPA),

wherein said ICs are coupled in series between said first power source line and said current source in such a manner that the second terminal of a preceding one of said ICs is connected to the first terminal of a succeeding one of said ICs (fig. 1 VDD cascaded 1,2,3,4 and (5) AAPA),

wherein at least one of said plurality of current-drive ICs produces an internal reference voltage (fig. 1 R2 Yatabe) based on a voltage at both ends of said first resistor(fig. 1 R2 Yatabe).

6. In regards to claim 6, AAPA fails to teach the current-drive apparatus according to claim 1, wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a high voltage supply and a plurality of second operational amplifiers, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply, and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current.

However, Yatabe teaches a system and method for wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier (fig. 1 2a), provided as a voltage follower (fig. 1 (2a) voltage follower), for outputting a voltage appearing at a terminal of said reference resistor (**fig. 1 R1-R5**) on the side of a high voltage supply (fig. 1 (VDD)) and a plurality of second operational amplifiers (fig. 1 (2b)), provided as a voltage follower (fig. 1 (2b) voltage follower), for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply

Art Unit: 2629

(fig. 1 VEE), and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current ((fig. 1 R8,R9, R10 and R11 is applied to both terminals col. 7, lines 1-30 of Yatabe).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA to include the use of wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a high voltage supply and a plurality of second operational amplifiers, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply, and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current as taught by Yatabe in order to provide a means to reduce the potential difference between the two driving potentials and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as as stated in (col. 4, lines 25-47 of Yatabe).

Art Unit: 2629

7. In regards to claim 7, AAPA as modified by Yatabe teaches the current-drive apparatus according to claim 6, wherein said at least one of said plurality of current-drive circuits further includes a reference current part (fig. 1 C5 and C6 of Yatabe)) disposed between each of said of current adjustment resistor and said low voltage supply (fig. 1, R8, R9, R10 and R11 and VEE of Yatabe), and is configured so that an output of corresponding one of said plurality of second operational amplifiers is input to said reference current part in order to allow said corresponding one of said at least one internal reference current to flow to said low voltage supply (fig. 1 through OP4 through C4 the smoothing capacitor of Yatabe).

8. In regards to claim 28, AAPA fails to teach the system as claimed in claims 25, wherein at least one of said plurality of current-drive ICs further includes:

- a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof;

- a second OP amplifier having an input coupled to a node between said second terminal and said and said first resistor and an output thereof; and

- wherein the second resistor is coupled between the outputs of said first and second OP amplifiers.

However, Yatabe teaches wherein at least one of said plurality of current-drive ICs further includes (abstract):

- a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof (fig. 1 OP1);

a second OP amplifier having an input coupled to a node between said second terminal and said and said first resistor and an output thereof (fig. 1 OP2); and

wherein the second resistor is coupled between the outputs of said first and second OP amplifiers (fig. 1 R9 examiner notes one end of resistor R9 is connected between the outputs V1 and V2).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA to include the use of a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof; a second OP amplifier having an input coupled to a node between said second terminal and said and said first resistor and an output thereof; and wherein the second resistor is coupled between the outputs of said first and second OP amplifiers as taught by Yatabe in order to provide a means to reduce the potential difference between the two driving potentials and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as as stated in (col. 4, lines 25-47 of Yatabe).

9. In regards to claim 29, AAPA as modified by Yatabe teaches the current-drive apparatus according to claim 1, wherein said current-drive circuit is operable to sum up the at least one internal reference current in a desired number and output a desired number of internal reference currents to a display element of said display panel (col. 10, lines 39-65 Yatabe).

Response to Arguments

10. Applicant's arguments, see Remarks, filed 6/28/2010, with respect to R12 and R13 have been fully considered and are persuasive.

However, Yatabe teaches, voltage dividing resistors R1-R5 and states, "[t]he outputs of operational amplifiers OP1, OP2, OP3 and OP4 are output via resistors R8, R9, R10 and R11 which are used to limit the output current of the operational amplifiers, and the output electric potentials V1, V2, V3 and V4, along with the power source electric potentials VDD=V0 and VEE=V5, are supplied to the driving circuit of a liquid crystal panel (not shown). Here, smoothing capacitors C1, C2, C3 and C4 are respectively connected between the output electric potentials V0 and V1, V1 and V2, V3 and V4 and V4 and V5. " (6) Between the power source electric potentials VDD and VEE, a voltage dividing circuit S is connected in parallel with the circuit composed of the above-described voltage dividing resistors R1, R2, R3, R4 and R5. (col. 7, lines 11-23).

Examiner notes that Applicant's specification states, "[t]he reference resistor R_r is connected between terminals 101 and 102 of each of the current-drive ICs IC1 to IC4 to-divide the high voltage supply VDD into a plurality of voltages (refer to FIG. 4)" [0052] PG PUB. Similarly, Yatabe uses R2 as a voltage divider from the high voltage supply VDD before being applied to a voltage follower. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA to include the use of a reference resistor as taught by Yatabe such that "it is possible for the electric potential difference between the two driving electric potentials which are supplied to the output circuit to be reduced more than the electric potential difference between a first electric

Art Unit: 2629

potential and a second electric potential, and consequently, it is possible to reduce the voltage resistance of the circuit device of the output circuit, and also to reduce the power consumption via the output circuit” as stated in (col. 4, lines 37-43 of Yatabe).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629